Notice of Allowability	Application No.	Applicant(s)	
	10/826,198	BREWER, SIMON	
	Examiner	Art Unit	
	Linda Wong	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 12/14/2006*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
2. Authorization for this examiner's amendment was given in a telephone interview with Mikio Ishimaru on 3/6/2007.
3. The application has been amended as follows:

   a. Claim 1, (currently amended) A method for measuring jitter on a data signal, comprising:

   inputting a data signal under test to digitally generate at least one data signal transition ~~locations~~ location in ~~the~~ delay elements of a delay line;

   determining ~~the~~ ΔT time delays of the delay elements without using ~~a~~ the data signal under test;

   digitally latching ~~a~~ the data signal transition location using a stable sampling clock signal and only the output of the delay line;

   digitally converting the latched data signal transition location to a delay time value output that is the ΔT time delays of the corresponding delay elements;

   digitally converting the delay time value to an edge position output; and

   digitally detecting a value of the edge position output.

   b. Claim 6, (currently amended) A method for measuring jitter on a data signal, comprising:

inputting a data signal under test to digitally generate at least one data signal transition ~~locations~~ location in ~~the~~ elements of a delay line;

determining ~~the~~ ΔT time delays of the delay elements without using ~~a~~ the data signal under test;

digitally latching a the data signal transition location using a stable sampling clock signal and only the output of the delay line;

digitally converting the latched data signal transition location to a delay time value output that is the ΔT time delays of the corresponding delay elements;

digitally converting the delay time value to an edge position output using the sampling clock signal;

digitally detecting peak-to-peak values of the edge positions; and

outputting the detected peak-to-peak values of the edge positions.

c. Claim 11. (currently amended) Apparatus for measuring jitter on a data signal, comprising:

a tapped delay line having delay elements for digitally generating at least one data signal transition ~~locations~~ location therein from a data signal under test inputted thereinto;

circuitry including a calibrator for determining the ΔT time delays of the delay elements without using a data signal under test;

a stable sampling clock signal;

a sample register connected for digitally latching ~~a~~ the data signal transition

location therein in response to the stable sampling clock signal and only the output of the delay line;

a priority encoder connected for digitally converting the latched data signal transition location to a delay time value output that is the ΔT time delays of the corresponding delay elements;

a converter connected for digitally converting the delay time value output to an edge position output; and

a peak-to-peak detector connected for digitally detecting values of the edge positions.

d. Claim 16. (currently amended) Apparatus for measuring jitter on a data signal, comprising:

a field programmable gate array carry chain;

a tapped delay line having delay elements, that is implemented in the field programmable gate array carry chain for digitally generating at least one data signal transition ~~locations~~ location therein from a data signal under test inputted thereinto;

circuitry including a calibrator for determining the ΔT time delays of the delay elements without using a data signal under test;

a stable sampling clock signal;

a sample register connected for digitally latching ~~a~~ the data signal transition location therein in response to the stable sampling clock signal and only the output of the delay line;

a priority encoder connected for digitally converting the latched data signal transition location to a delay time value output that is the ΔT time delays of the corresponding delay elements;

a converter for digitally converting clock and delay time value output to time values and connected for digitally converting the delay time value output to an edge position output; and

a peak-to-peak detector connected for digitally detecting and outputting peak-to-peak values of the edge positions.

4. The following changes to the drawings have been approved by the examiner and agreed upon by applicant: Replacement drawings indicating the changes are attached. In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

5. The following is an examiner's statement of reasons for allowance: The claimed limitation refers to a method and apparatus for determining the amount of jitter by delaying a data signal using a delay line with delay elements, determining the time delay without using a data signal, latching the data signal transition locations outputted from the delay line, converting the data signal transition locations to a delay time value, converting the delay time value to an edge position and detecting a value of the edge position. Prior art searched, in combination or alone, fails to disclose all the limitations as stated in the claims.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong
3/6/2007

KEVIN KIM
PRIMARY PATENT EXAMINER

Title: METHOD AND APPARATUS FOR MEASURING JITTER
Inventor: Symon Brewer
Docket No.: 21-014
Contact: Mikio Ishimaru (408) 738-0592

REPLACEMENT

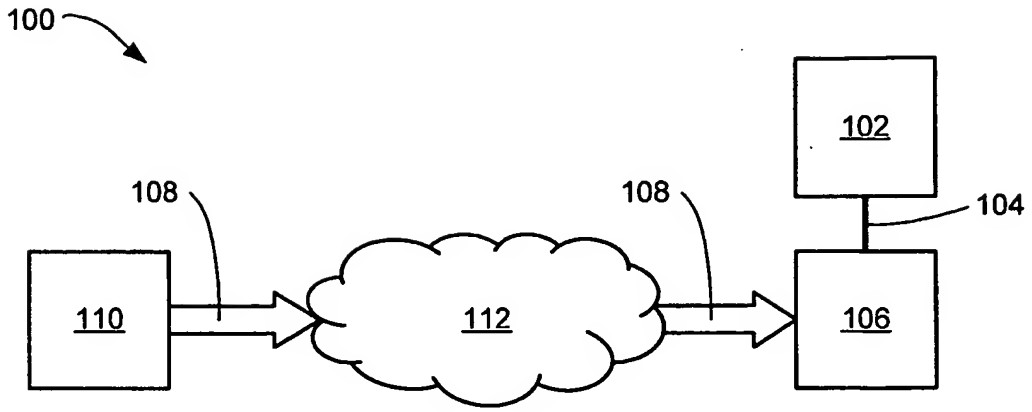

FIG. 1

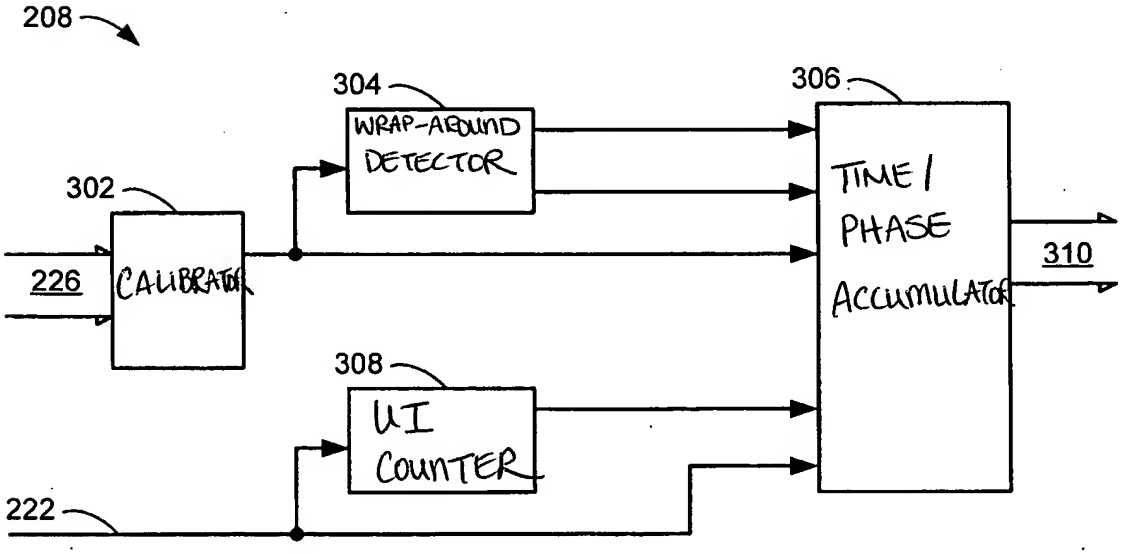

FIG. 3

REPLACEMENT

2/3

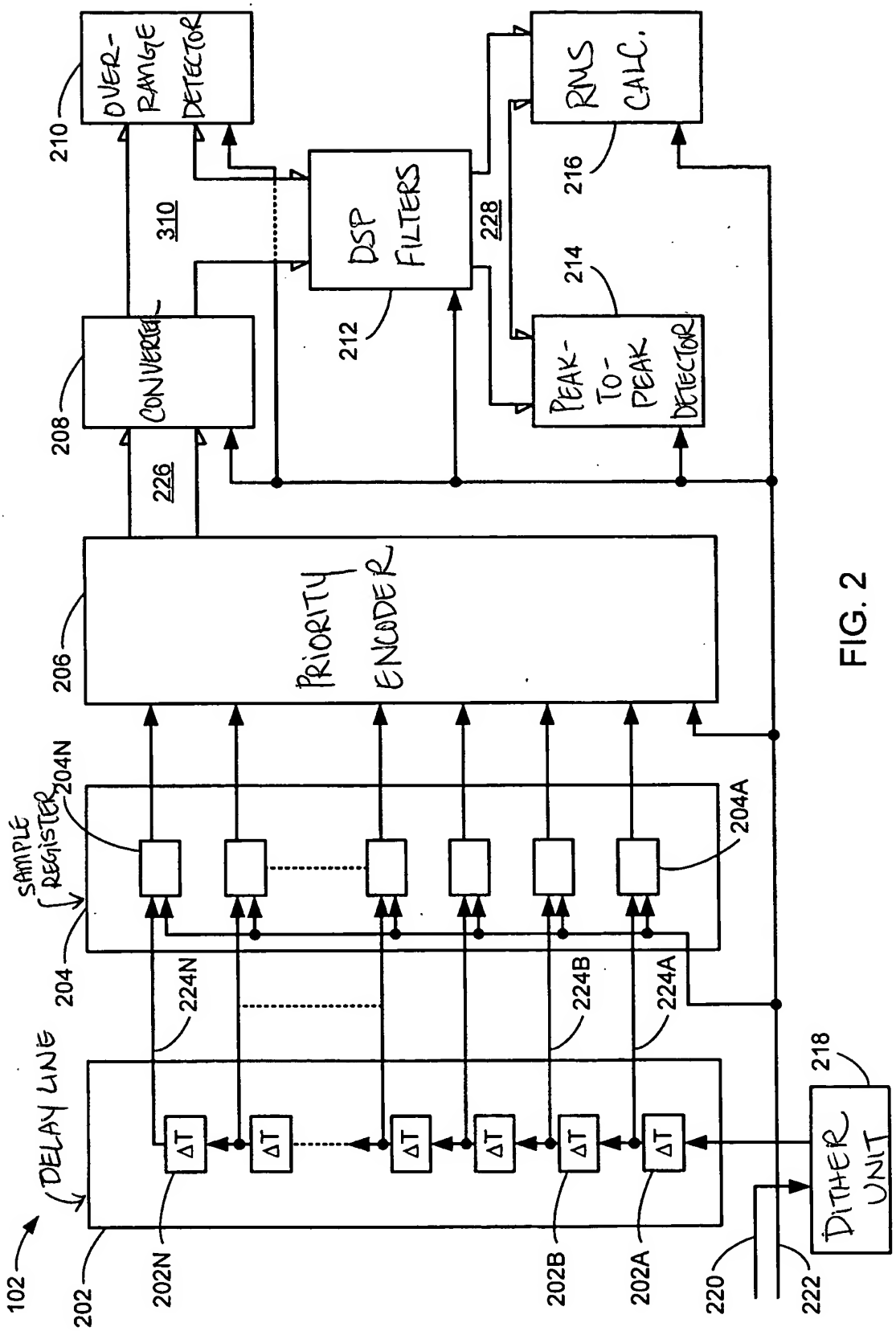

FIG. 2

Title: METHOD AND APPARATUS FOR MEASURING JITTER
Inventor: Symon Brewer
Docket No.: 21-014
Contact: Mikio Ishimaru (408) 738-0592

REPLACEMENT

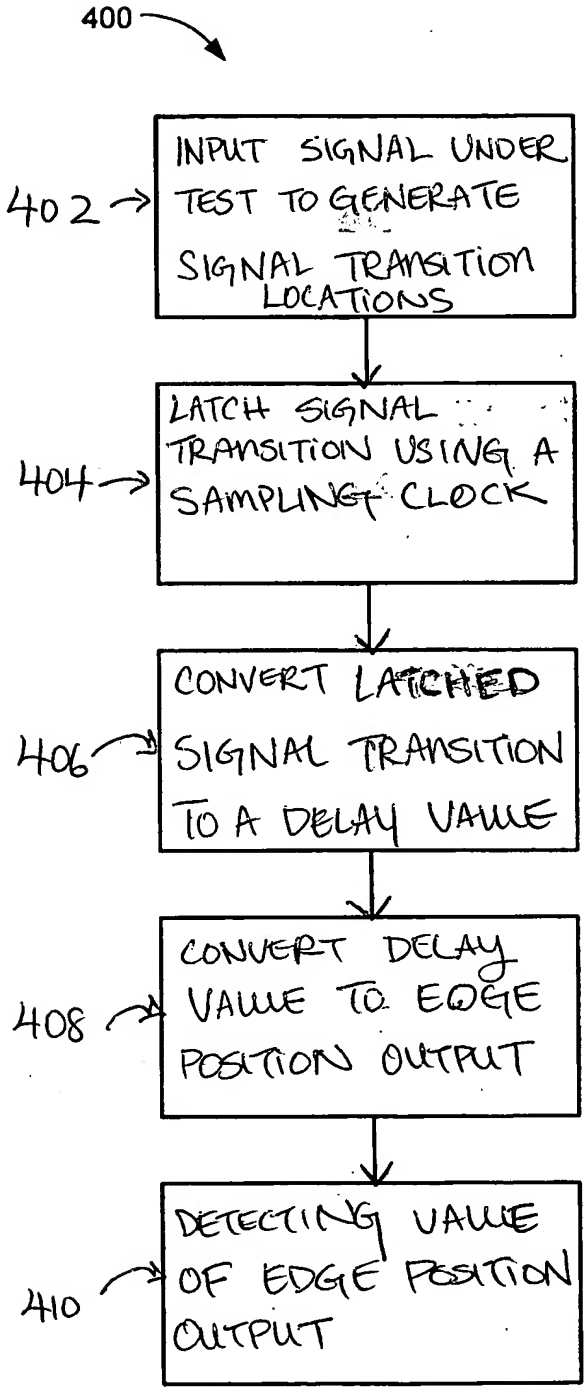

FIG. 4